



Institut de Microélectronique, Electromagnétisme et Photonique

IMEP-LAHC, Grenoble INP, BP 257

MINATEC

38016 Grenoble cedex 1, France

PhD Position

Topic: *Characterization and modeling of Si and III-V FET devices under deep cryogenic condition*

Start: January 2020

Salary: 1400 EUR / month (net)

Context

Quantum computing is currently attracting a lot of research due to its high potential for complex calculation and cryptography applications. The core elements of quantum computing are Qbits, but they must be addressed and accessed using an embedded CMOS technology, which hence needs to operate at very low temperatures, as Qbit devices only operate in cryogenic conditions. The understanding of MOSFET operation at very low temperature is well known since the 90s, but modern and emerging technologies like FDSOI, FinFET, III-V HEMT or NanoWire, which will be needed in the framework of quantum computing, have not been extensively studied at low temperature. One particular property of these technologies is their high surface to volume ratio and their use of high-K materials, which may lead to an undesired increased impact of electronic noise, related to the presence of traps and defects, extremely detrimental for quantum computing. In addition, MOSFET devices generate heat, which impacts their own operation, in a phenomenon called the Self Heating Effect (SHE). This effect is still not fully understood yet, especially at low temperature. Therefore, the cryogenic behavior of these new MOSFET architectures has to be fully re-investigated in the light of their future use for quantum computing application.

In order to face these exciting challenges and in the framework of this proposed PhD subject, the student will **perform a detailed experimental study of Si and III-V FET electrical properties and reliability in cryogenic conditions (down to 4K), using the state-of-the-art facilities of IMEP-LAHC**. This work will then be followed by the development of physical models, which will be used by teams of circuit designers, in the framework of a European project (SEQUENCE) whose general objectives are:

- To provide technology for scalable cryogenic electronics supporting emerging quantum computing technologies.
- To mature a selected set of emerging device technologies with technology benchmark to support future technology nodes.
- To establish the optimal balance between III-V, Si CMOS, and other emerging device technologies to meet the special requirements of cryogenic electronics.

Detailed overview of the PhD subject

1. Advanced cryogenic electrical characterization

The PhD student will perform a detailed electrical characterization from room temperature down to 4K, on various Si and III-V MOS devices, fabricated by the partners of SEQUENCE (LETI/CEA, Lund University, IBM Zurich). The challenges include proper assessment of electrical properties of devices through Capacitance-Voltage and Current-Voltage measurements on devices featuring short gate length and small width (nanometrics sizes). Magneto-transport measurements down to 4K and up to 9 Teslas will also be carried out to evaluate more precisely the channel transport mechanisms by Hall Effect and magnetoresistance phenomena.

2. Interface and dielectric trap characterization

The PhD student will perform a refined analysis of the device gate dielectric-channel interface quality based on low frequency noise (LFN), random telegraph noise (RTN) and Charge Pumping (CP) measurements. The origin of different noise sources will be identified, aiming in the proper trap parameter extraction and noise modeling. In small area devices in particular, the onset of RTN will be investigated for comparison to the usual 1/f (flicker) noise and additionally provide single defect characteristics.

3. Self-heating effect characterization

The PhD student will carry out SHE electrical characterization by specific pulsed I-V measurements on various selected devices in order to benchmark different device architectures and technologies. The techniques of gate thermometry and thermal microscopy may also be examined.

4. Modelling and simulation

The PhD student will also conduct a physical modelling of the operation of such Si/III-V FET devices based on Poisson-Schrodinger simulation carried out at deep cryogenic temperatures. She/he will focus both on charge and capacitance characteristics, transport properties as well as on low frequency noise modelling, in order to better interpret the experimental data on one hand, and examine the device behavior in a circuit, through Verilog-A model development.

Environment

IMEP-LAHC (MINATEC) benefits from a renowned expertise in low temperature characterization and modelling of CMOS devices since the end of 80s, with emphasis on MOSFET parameter extraction, LF noise and transport in inversion layer at cryogenic temperatures for space applications. IMEP-LAHC has also founded the workshop on low temperature electronics (WOLTE) in 1994, still running today. In the framework of the European project SEQUENCE, IMEP-LAHC will contribute to the characterization and modeling of Si and III-V MOS devices fabricated at LETI/CEA (Grenoble), Lund University (Sweden) and IBM Zurich (Switzerland).

Required student profile

The student should have knowledge of electronics and semiconductor physics, as well as basic understanding of semiconductor device operation principles and applications. Technical skills regarding data treatment through Origin, MATLAB, Mathcad or Python will be needed. Already acquired experience in electrical characterization will be appreciated.

Contact

PhD supervisor

Prof. *Francis Balestra*, CNRS director of research, francis.balestra@grenoble-inp.fr

PhD co-supervisor

Dr. *Christoforos Theodorou*, CNRS researcher, christoforos.theodorou@grenoble-inp.fr (+330456529549)