IMEP-LAHC

SEMINAIRE

(de 13 h à 14 h, amphithéâtre PHELMA, Bât. INP, MINATEC,
ouvert aux chercheurs des autres laboratoires)

Jeudi 8 décembre 2011

"Challenges of ESD RF protections in advanced CMOS technologies"

par Philippe GALY

Abstract: The main purpose of this presentation is to discuss the challenge of RF ESD protections for the Advanced CMOS technologies. Today, it is well known that the ElectroStatic Discharge (ESD) protection is already a major challenge. This is due to the complexity of the technologies (High K metal Gate, sub-nanometric size, dual oxide…) and due to the complexity of System On Chip (SOC) (Mono-multi dice, multi powers, multi applications, multi balls …). After a short introduction on the technology Roadmap and SOC complexity, the ESD constraints are introduced. At this step, the main accent will be done on the integration context challenge. Afterwards, the focus will be on RF constraints coupled with ESD protections. Some approaches, results and silicon implementations are presented and evaluated.

Philippe Galy *is Senior Expert in micro-nano electronics at STMicrolectronics R&D Crolles France since 2005. He manages 4 groups in the Advanced Device Design & ESD Solutions (ADDES) team. Before, he was professor in engineer school during 10 years old. He has authored or co-authored more than 75 publications, 2 books and 20 patents. He holds a Ph.D. and H.D.R. (academic research supervisor).*

Institut de Microélectronique, Electromagnétisme et Photonique
MINATEC, INPG, 3 Parvis Louis Neel, BP 257, 38016 GRENOBLE CEDEX 1, France
Tél. +33 (0) 456.529.503 - Fax. +33 (0) 456.529.501
UMR 5130 CNRS INPG UJF
Institut Polytechnique de GRENOBLE