



SEMINAIRE

(de 13 h à 14 h, amphithéâtre PHELMA, Bât. INP, MINATEC,
ouvert à tous : enseignants, étudiants, chercheurs, administratifs, techniciens)
Jeudi 7 mai 2015

“Resistive memories embedded in advanced logic CMOS technologies”
par Elisa VIANELLO
(CEA- LETI)

Abstract: The application potential of the new emerging resistive memories - as metal oxide resistive switching memory (OxRAM) or conductive-bridge memory (CBRAM) - covers the standalone memory technologies (as NAND and DRAM), but offers also potential for exciting new applications and markets, as new functionality coupled with logic circuits to enable block power-down, or use as synapses in neuromorphic circuits.

In this presentation, we briefly present different ReRAM technologies, OxRAM, CBRAM developed in the Memory Component Laboratory in Leti. Moreover we will focus on the role that the different resistive memory technologies can play in new emerging fields of applications. Concerning the introduction of non-volatile functionality at the logic level, we will demonstrate hybrid (CMOS logic + ReRAM devices, specifically CBRAM and OXRAM) circuits for Ultra Low Power (ULP) FPGA and fixed-logic IC design (as Non Volatile Flip-Flops). Concerning neuromorphic circuits, we will focus on the emulation of synaptic plasticity effects with resistive memories synapses (specifically, OxRAM or CBRAM). We will show the implementation of large-scale energy efficient neuromorphic systems with stochastic-binary synapses.

Elisa Vianello received the B.S. and M.S. in electronic engineering, with microelectronics specialization (2006), from the Università degli Studi di Udine. She received the Ph.D. degree in micro- and nano-electronics from INPG and the Università degli Studi di Udine (Italy) (2009), working on modeling and electrical characterization of charge trapping non volatile memory cells. She joined Fondazione Bruno Kessler (www.fbk.eu) – Micro Technologies Laboratory (MTLab), Trento, Italy as a research engineer in 2009 where she was working on the development of Silicon radiation detectors: 3D Double-sided Double-Type Column (3D-DDTC) detectors for the upgrade of the Large Hadron Collider at the CERN (Genève). Since 2011 she is scientist at CEA-LETI Grenoble. She is in charge of the “Oxide Based Resistive RAM” activity in the memory lab. Her current research interests concern the electrical characterization, processing, engineering of innovative resistive memory devices and new computing paradigms beyond von-Neumann architecture with focus on the brain-inspired neuromorphic computing. She is author or co-author of more than 50 technical papers. She is a reviewer of several international journals (IEEE Elec. Dev. Let., IEEE Trans. on Electr. Dev., Solid State Elec., Mic. Reliability...). She was in the technical committee of the International Reliability Physics Symposium IRPS “Memory Technology” subcommittee (2013-2014).

*Institut de Microélectronique, Electromagnétisme et Photonique
MINATEC, Grenoble-INP, 3 Parvis Louis Neel, CS 50257, 38016 GRENOBLE CEDEX 1, France
Tél. +33 (0) 456.529.503 - Fax. +33 (0) 456.529.501
UMR 5130 CNRS Grenoble-INP UJF
Institut Polytechnique de GRENOBLE*