



SEMINAIRE

(de 13 h à 14 h, amphithéâtre PHELMA, Bât. INP, MINATEC,
ouvert aux chercheurs des autres laboratoires)

Jeudi 9 janvier 2014

“Vertical heterojunction Tunnel FETs based on
transition metal dichalcogenides”

by David ESSENI

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Abstract: In this presentation I will first introduce the context of the so-called power crisis that well describes the present stage of the development of computation technologies. In fact most of the digital systems around us today are power limited, and their performance is essentially the best that it can be obtained with the available power or energy budget. The scaling of the supply voltage is the most effective measure to improve the energy efficiency of CMOS device and circuits, and the development of small slope switches (i.e. transistors having a sub-threshold swing better than 60mV/dec) is a relevant and timely topic. In this framework, I will then briefly introduce the basic properties of transition metal dichalcogenides (TMD) MX₂ (M = Mo, W and X = S, Se), which form a family of quasi-2D crystals having an energy band-gap typically ranging between 1eV and 2eV.

I will show that TMD monolayers offer a variety of valence to conduction band alignments, ranging from staggered to broken bandgap, that can be used to in a vertical hetero-junction Tunnel FET with great potentials to achieve a very abrupt turn on characteristic. In this regard, I will show some preliminary calculations of the current-voltage characteristic of such devices obtained by using a semi-classical, transfer-Hamiltonian methodology, and then propose an outlook about future work dealing with the modeling and with the practical implementation of such tunneling transistors.

David Esseni received PhD from the University of Bologna in 1999 and is currently Professor at the University of Udine, Italy. During year 2000 he was a visiting scientist at Bell Labs-Murray Hill (NJ) - Lucent Technologies and in 2013 he was Fulbright Research Scholar at the University of Notre Dame (IN). His research interests include the characterization, modeling and design of CMOS and beyond CMOS transistors and of non-volatile memories. He has served or is serving as a member of the technical committee of the International Electron Devices Meeting (IEDM), the European Solid-State Device Research Conference (ESSDERC), and the International Reliability Physics Symposium (IRPS). D. Esseni is an Associate Editor of the IEEE Transactions on Electron Devices (IEEE-TED) and a Fellow of the IEEE Electron Devices Society.