infos'11

INSULATING FILMS ON SEMICONDUCTORS

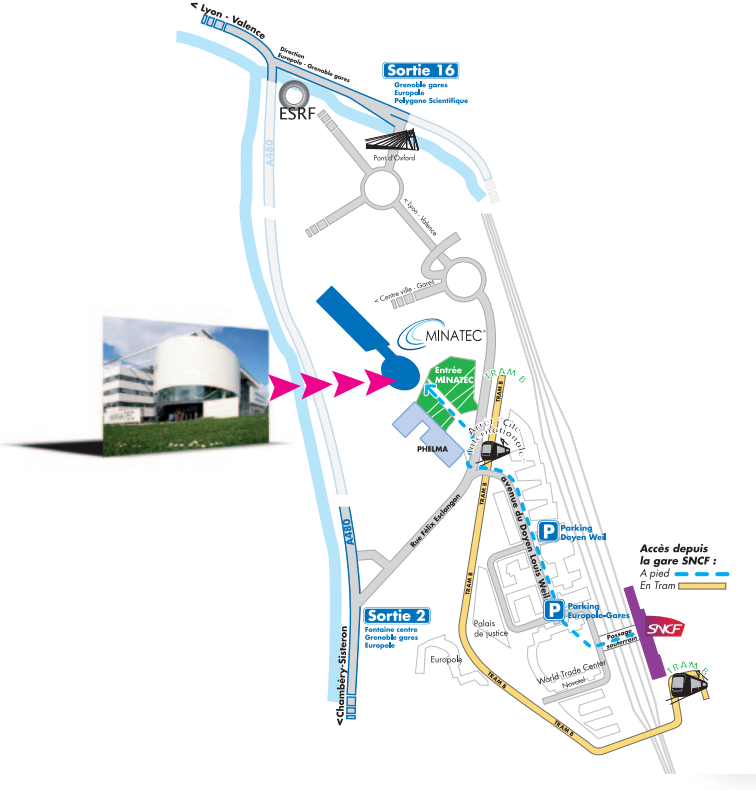
17th International Conference

Final program

Grenoble
June 21-24, 2011

Maps


"Maison MINATEC - MINATEC Meeting Center"
Accueil évènement
Accueil MINATEC
Entrée évènement
Chapiteau évènement
Régie auditorium
Auditorium
Salle de réunion
Salle de réunion
Salle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Direction Europole - Grenoble gares
Sortie 16
Grenoble gares
Europole
Polygone Scientifique
ESRF
A480
Pont d'Oxford
< Lyon - Valence
< Centre ville - Gares
MINATEC
Entrée MINATEC
TRAM B
PHELMA
Avenue Centrale
Avenue du Doyen Louis Weil
Rue Félix Esclangon
A480
Parking Doyen Weil
Parking Europole-Gares
Accès depuis la gare SNCF :
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Palais de justice
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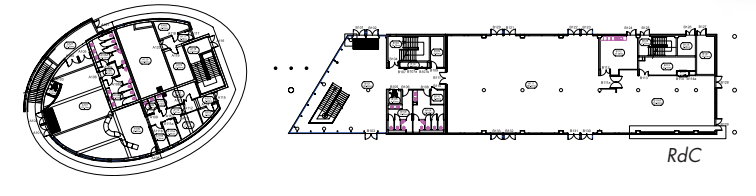
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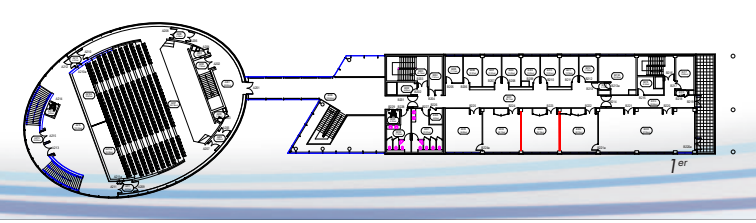
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Welcome to Grenoble

Microelectronics is entering a new era where novel concepts, materials and devices are expected to play an increasing role. Nanoelectronics is already around the corner ready to take the relay. Alternative semiconductors, dielectrics and related interfaces are coming into the arena, contesting the despotic leadership of silicon and silicon dioxide. The merits of these non-Si/SiO_2 candidates are examined and debated at INFOS conference.

INFOS is designed as an international forum for promoting high-level scientific research and exchanges between research groups and industrial partners involved, all over the world, in dielectrics, semiconductors, thin films and interfaces. Following its lively experience and ground rules, INFOS 2011 features oral and poster sessions, key-note presentations, a training course as well as informal discussions. INFOS covers recent progress in several areas of interest, including: (i) high-K dielectrics, metal gates, high mobility substrates (Ge, SiGe, GaN, III-V), (ii) dielectrics for nonvolatile, DRAM, resistive switching and spin memories, (iii) semiconductors on insulators, (iv) dielectrics for nanowires, 3D devices and carbon-based devices, (v) surface cleaning, physics and chemistry of dielectrics and defects, characterization techniques, reliability, (vi) electronic structure theory, ferroelectrics and functional oxides, (vii) dielectrics and thin materials for TFTs, amorphous or organic devices, etc.

Following the great success of the recent editions in Barcelona (2003), Leuven (2005), Athens (2007) and Cambridge (2009), Grenoble has been selected to organize the 17th edition. The tradition and prestige of INFOS conferences come from the high quality of contributed and invited papers. We have received 160 submissions. The final program includes 15 invited talks, 66 oral presentations and 49 posters. Illustrious speakers have been invited to share their experience in multiple domains; Dr Kelin Kuhn from INTEL is our special guest. The participants will benefit from a wide-angle view of the current landscape of micro-nano science and technology. INFOS'11 also features a tutorial on 'new challenges in nanoelectronics', a very timely and important topic as CMOS is capturing new markets. The lectures are given by word-leading experts and explore new opportunities.

Grenoble is a high-tech city, with wonderful surroundings in the heart of the Alps, offering attractive tourism opportunities over the weekend. The participants are warmly invited to slightly extend their stay, from June to December, such as to enjoy skiing …

It is our duty and great pleasure to thank the authors for their contributions and the members of the Technical/Steering/Organizing Committees for their enthusiastic work. Our sponsors are sincerely acknowledged for their generous contributions. Looking forward to a successful conference, with exciting scientific contents and rich human interactions, we warmly welcome you in Grenoble.

Sorin Cristoloveanu & Gilles Reimbold
INFOS'11 Chairs

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(IMEP & LETI at MINATEC)

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Tuesday June 21, 2011

07:30-08:30 Registration at PHELMA entrance (MINATEC site)

TUTORIALS 'New Challenges in Nanoelectronics'
(PHELMA hall)

Tutorials Chair: G. Ghibaudo

08:30-08:40 **Opening**

08:40-09:40 **High mobility channels for advanced CMOS**
A. Dimoulas (NCSR, Demokritos, Athens, Greece)

09:40-10:10 Coffee break

10:10-11:10 **Physical trends of high-k oxides: report from a tour in the Periodic System**
O. Engstrom (Chalmers University, Sweden)

11:15-12:15 **Recent trends in CMOS front-end reliability**
B. Kaczer (IMEC, Leuven, Belgium)

12:15-14:00 Lunch at Restaurant "Le Carré"

14:00-15:00 **Silicon non volatile memories: Paths of innovation**
B. DeSalvo (LETI-CEA, Grenoble, France)

15:05-16:05 **Nano characterization of materials**
D. Schroder (Arizona State University, USA)

16:05-16:35 Coffee break

16:35-17:35 **Advanced modelling and simulations approaches**
G. Baccarani (Bologna University, Italy)

Wednesday June 22, 2011

07:30-08:30 Registration at MINATEC entrance

Room A Plenary Session

Session Chairs: S. Cristoloveanu & G. Reimbold

08:30 Conference opening

08:40 KEYNOTE: Kelin J. Kuhn, *Intel Corporation, Hillsboro, U.S.A.*
Moore's crystal ball: device physics and technology past the 15nm generation

09:25 INVITED: **Materials and Process Aspect of Cross-Point RRAM**
J. Lee[1], M. Jo[1], D.-J. Seong[1], J. Shin[1], Hyunsang Hwang[1,2]
[1]School of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju, South Korea, [2]Department of Nanobio Materials and Electronics, Gwangju Institute of Science and Technology, Gwangju, South Korea.

10:05-10:25 Coffee break

Room A Session 2a: III-V interfaces (1)

Session Chairs: M. Heyns & S. Hall

10:25 **Band offsets at the (100)GaSb/Al_2O_3 interface from internal electron photoemission study**
V.V. Afanas'ev[1], H.-Y. Chou[1], A. Stesmans[1], C. Merckling[2], and X. Sun[3]
[1]Department of Physics and Astronomy, University of Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium, [2]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, [3]Department of Electrical Engineering, University of Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium and Department of Electrical Engineering, Yale University, New Haven, CT 06520, USA.

10:45 **The structural and electrical properties of the $SrTa_2O_6/In_{0.53}Ga_{0.47}As$/InP system**
P.F. Zhang, R.E. Nagle, N. Deepak, I.M. Povey, Y.Y. Gomeniuk, E. O'Connor, N. Petkov, M. Schmidt, T.P. O'Regan, K. Cherkaoui, M.E. Pemble, P.K. Hurley, R.W. Whatmore
Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland.

11:05 **Direct measurement of interfacial structure in epitaxial Gd_2O_3 on GaAs (100) using scanning tunneling microscopy**
Y. P. Chiu[a], M. C. Shih[a], B. C. Huang[a], J. Y. Shen[b], M. L. Huang[c], W. C. Lee[c], P. Chang[b], T. H. Chiang[b], M. Hong[b], and J. Kwo[c,d]

[a]Department of Physics, National Sun Yat-Sen University, Kaohsiung, 80424, Taiwan, [b]Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, 30013, Taiwan, [c]Department of Physics, National Tsing Hua University, Hsinchu, 30013, Taiwan, [d]Center for Condensed Matter Sciences, National Taiwan University, Taipei, 10617, Taiwan.

11:25 **Is interfacial chemistry correlated to gap states for high-k/III-V interfaces?**

W. Wang, C. L.Hinkle, E. M. Vogel, K. Cho and R. M. Wallace
Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, Texas 75080, USA.

11:45 **1.2 nm capacitance equivalent thickness gate stacks on Si-passivated GaAs**

M. El Kazzi, D. J. Webb, L. Czornomaz, C. Rossel, C. Gerl, M. Richter, M. Sousa, D. Caimi, H. Siegwart, J. Fompeyrine, and C. Marchiori
IBM Research – Zurich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland.

12:05-13:40 Lunch

Room B Session 2b: Resistive memories

Session Chairs: L. Larcher & J. Klootwijk

10:25 **Filament diffusion model for simulating reset and retention processes in RRAM**

S. Larentis, C. Cagli, F. Nardi and D. Ielmini
Dipartimento di Elettronica e Informazione (DEI) – Politecnico di Milano and IUNET, Milano, Italy.

10:45 **Evidence for compliance controlled oxygen vacancy and metal filament based resistive switching mechanisms in RRAM**

N. Raghavan[a], K. L. Pey[a, b], W. Liu[a], X. Wu[a], X. Li[c] and M. Bosman[d]
*[a]School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore 639 798. [b]Singapore University of Technology and Design (SUTD), Singapore 279 623. [c]A*STAR Institute of Microelectronics (IME), Science Park II, Singapore 117 685. [d]A*STAR Institute of Materials Research and Engineering (IMRE), Singapore 117 602.*

11:05 **Accurate analysis of parasitic current overshoot during forming operation in RRAMs**

S. Tirano[1,2], L. Perniola[1], J. Buckley[1], J. Cluzel[1], V. Jousseaume[1], Ch. Muller[2], D. Deleruyelle[2], B. De Salvo[1], G. Reimbold[1]
[1]CEA-LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 Grenoble, France, [2]IM2NP, UMR CNRS 6242, Aix-Marseille Université, F-13451 Marseille Cedex 20, France.

11:25 **Resistive switching characteristics of CMOS embedded HfO_2-based 1T1R cells**

D. Walczyk[a], Ch. Walczyk[a], T. Schroeder[a], T. Bertaud[a], M. Sowińska[a], M. Lukosius[a], M. Fraschke[a], B. Tillack[a,b], and Ch. Wenger[a]

[a]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany, [b]Department of Computer Engineering and Microelectronics, Technische Universität Berlin, 10587 Berlin, Germany.

11:45 **Resistive switching characteristics of ultra-thin TiO_x**

J. Park[1], S. Jung[1], J. Lee[1], W. Lee[1], S. Kim[1], J. Shin[1], and H. Hwang[1, 2]

[1]Department of Material Science and Engineering, [2] Department of Nanobio Materials and Electronics, Gwangju Institute of Science and Technology, Gwangju 500-712, Korea.

12:05-13:40 Lunch

Room A Session 3a: III-V devices

Session Chairs: K. Kuhn & S. Mantl

13:40 INVITED: **III-V nMOSFETs - some issues associated with roadmap worthiness**

I. Thayne[1], S. Bentley[1], M. Holland[1], W. Jansen[1], X. Li[1], D. Macintyre[1], S. Thoms[1], B. Shin[3], J. Ahn[2], P. McIntyre[2]

[1]Nanoelectronics Research Centre, University of Glasgow, Glasgow, UK, [2]Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305 USA, [3]B. Shin Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305, USA; now at IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA.

14:20 **On the mechanisms limiting mobility in InP/InGaAs buried channel nMISFETs**

Y. Urabe[a], T. Yasuda[a], H. Ishii[a], T. Itatani[a], N. Miyata[a], H. Yamada[a], N. Fukuhara[b], M. Hata[b], M. Takenaka[c], S. Takagi[c]

[a]National Institute of Advanced Industrial Science and Technology (AIST), 1-1-1 Higashi, Tsukuba, Ibaraki 305-8562, Japan, [b]Sumitomo Chemical, 6 Kitahara, Tsukuba, Ibaraki 300-3294, Japan, [c]The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan.

14:40 **Mobility spectrum analysis of anisotropic electron transport in N-polar GaN/AlGaN heterostructures on vicinal sapphire substrates**

G.A. Umana-Membreno[a], T.B. Fehlberg[a], S. Kolluri[b], D.F. Brown[b], G. Parish[a], B.D. Nener[a], S. Keller[b], U.K. Mishra[b], L. Faraone[a]

[a]School of Electrical, Electronic and Computer Engineering, The University of Western Australia, Crawley WA 6009, Australia, [b]Department of Electronic and Computer Engineering, University of California, Santa Barbara CA, USA.

15:00 **Remote phonon and surface roughness limited universal electron mobility of $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs**

A. M. Sonnet, R. V. Galatage, P. K. Hurley[¥], E. Pelucchi[¥], K. Thomas[¥], A. Gocalinska[¥], J. Huang[†], N. Goel[†], G. Bersuker[†], W. P. Kirk, C. L. Hinkle, and E. M. Vogel

The University of Texas at Dallas, Richardson, Texas 75080, USA, [¥]Tyndall National Institute, University College Cork, Ireland, [†]Sematech Inc., Austin, TX-78741, USA.

15:20-15:40 Coffee break

Room B Session 3b: Trap memories (1)

Session Chairs: G. Ghidini & D. Ielmini

13:40 **Effect of high temperature annealing on tunnel oxide properties in TANOS devices**

A. Arreghini, M. B. Zahid, G. Van den bosch, A. Suhane[1], L. Breuil, A. Cacciato and J. Van Houdt

Imec, Kapeldreef 75, B-3001 Leuven, Belgium, [1]also with ESAT, KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium.

14:00 **Enhanced operation and retention characteristics in charge-trapping flash memory device with a novel Si/Ge super-lattice channel**

L.-J. Liu, K.-S. Chang-Liao, Y.-C. Jian, and T.-K. Wang

Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan, R. O. C.

14.20 **Optimization of gate stack parameters towards 3D-SONOS application**

L. Breuil[1], G. Van den bosch[1], A. Cacciato[1], L. Date[2], G.S. Kar[1], B. Tang[1,3], A. Arreghini[1], I. Debusschere[1], J. Van Houdt[1]

[1]IMEC, Kapeldreef, 75, Leuven, Belgium; [2]Applied Materials Belgium; [3]Univ. Liverpool, UK.

14:40 INVITED: **Charge transport in high-k stacks for charge-trapping memory applications: a modeling perspective**

L. Larcher[1], A. Padovani[1,2], L. Vandelli[1], P. Pavan[3]

[1]DISMI, University of Modena and Reggio Emilia, via Amendola 2, Reggio Emilia, Italy, [2]InterMech Center, University of Modena and Reggio Emilia, via Amendola 2, Reggio Emilia, Italy, [3]DII, University of Modena and Reggio Emilia, Modena, Italy.

15:20-15:40 Coffee break

Room A Session 4a: III-V interfaces (2)

Session Chairs: J. Robertson & I. Thayne

15:40 **Molecular Beam Epitaxial study of InP(001)/GaSb/Al_2O_3 gate stack**

C. Merckling[1], X. Sun[2,3], A. Alian[1,2], T.Y. Hoffmann[1], M. Heyns[1,2], M. Caymax[1], J. Dekoster[1]

[1]Interuniversity Microelectronics Center (IMEC vzw), Kapeldreef 75, 3001, Leuven, Belgium, [2]Katholieke Universiteit Leuven, Celestijnelaan 200D, 3001, Leuven, Belgium, [3]Department of Electrical Engineering, Yale University, New Haven, CT 06520-8284, USA.

16:00 **AC response analysis of C-V curves and quantitative analysis of conductance curves in Al_2O_3/InP interfaces**

N. Taoka[1], M. Yokoyama[1], S. H. Kim[1], R. Suzuki[1], T. Hoshii[1], R. Iida[1], S. Lee[1], Y. Urabe[2], N. Miyata[2], T. Yasuda[2], H. Yamada[3], N. Fukuhara[3], M. Hata[3], M. Takenaka[1], and S. Takagi[1]

[1]The University of Tokyo, 7-3-1, Hongo, Bunkyo-ku, Tokyo 113-8656, Japan, [2]National Institute of Advanced Industrial Science and Technology, 1-1-1 Higashi, Tsukuba, Ibaraki 305-8562, Japan, [3]Sumitomo Chemical Co. Ltd., 6 Kitahara, Tsukuba, Ibaraki 300-3294, Japan.

16:20 **Interface composition of atomic layer deposited HfO_2 and Al_2O_3 thin films on InAs studied by X-ray photoemission spectroscopy**

R. Timm[a], M. Hjort[a], A. Fian[a], C. Thelander[a], E. Lind[a], J. N. Andersen[a], L. E. Wernersson[a,b], and A. Mikkelsen[a]

[a]Department of Physics, Lund University, 22100 Lund, Sweden, [b]Department of Electrical and Information Technology, Lund University, 22100 Lund, Sweden.

16:40 **Interface state densities, low frequency noise and electron mobility in surface channel $In_{0.53}Ga_{0.47}As$ n-MOSFETs with a ZrO_2 gate dielectric**

M. Adi Negara[1,2], N. Goel[3], D. Bauza[2], G. Ghibaudo[2], and P. K. Hurley[1]

[1]Tyndall National Institute, University College Cork, Lee Maltings, Cork, Ireland, [2]IMEP-LHAC, Minatec-INPG, BP 257, 38016 Grenoble, France, [3]SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, USA.

Room B Session 4b: Trap memories (2)

Session Chairs: H. Hwang & L. Selmi

15:40 **Stack engineering of TANOS charge-trap Flash memory cell using high-k ZrO_2 grown by ALD as charge trapping layer**

G. Congedo[1], A. Lamperti[1], L. Lamagna[1], and S. Spiga[1]

[1]Laboratorio MDM, IMM-CNR, via C. Olivetti 2, 20864 Agrate Brianza (MB) – Italy.

16:00 **Influence of metal gate and capping film stress on tanos cell performance**

M. Czernohorsky[1], T. Melde[3], V. Beyer[1], M.F. Beug[4], J. Paul[1], R. Hoffmann[1], R. Knöfler[2], and A.T. Tilke[2]

[1]Fraunhofer Center Nanoelectronic Technologies (CNT), 01099, Dresden, Germany, [2]Infineon Technologies Austria, 9500, Villach, Austria, [3]NaMLab gGmbH, 01187, Dresden, Germany, [4]Physikalisch Technische Bundesanstalt (PTB), 38116 Braunschweig, Germany.

16:20 **BE-TANOS: feasibility and technology limitations**

G. Ghidini, N. Galbiati, C. Scozzari, A. Sebastiani, R. Piagge, A. Del Vitto, P. Comite, M. Alessandri, P. Tessariol, L. Baldi, E. Moltrasio, E. Mascellino

Micron, R&D, 20041 Agrate Brianza, Italy.

18:30 **Poster Session and Reception at "La Bastille" fortress (by cable car)**

Thursday June 23, 2011

08:00-08:30 Registration at MINATEC entrance

Room A Session 5a: Theory (1)

Session Chairs: A. Pasquarello & J. Schubert

08:30 **Defects-induced gap states in hydrogenated γ-alumina used as blocking layer for non volatile memories**

L. Masoero[1], P. Blaise[1], G. Molas[1], J. P. Colonna[1], M. Gély[1], J. P. Barnes[1], G. Ghibaudo[2], B. De Salvo[1]

[1]CEA-LETI MINATEC, 38054 Grenoble Cedex 9, France, [2]IMEP-LAHC MINATEC, 38016 Grenoble Cedex 1, France.

08:50 **The role of oxygen-related defects and hydrogen impurities in HfO_2 and ZrO_2**

J. L. Lyons, A. Janotti, and C. G. Van de Walle

Materials Department, University of California, Santa Barbara, CA 93106-5050, USA.

09:10 **Shifting Schottky barrier heights with ultra-thin dielectric layers**

L. Lin[1], J. Robertson[1], and S. J. Clark[2]

[1]Engineering Dept, Cambridge University, Cambridge CB2 1PZ, UK, [2]Physics Dept, Durham University, Durham, UK.

09:30 **Atomic-scale theory on degradation of HfSiON gate stacks by atomic hydrogen accompanied by its interaction with oxygen vacancy and substitutional nitrogen**

Y. Nakasaki, I. Hirano, K. Kato, Y. Mitani

Toshiba Corporate R&D Centre, 1, Komukai-Toshiba-cho, Saiwai-ku, KAWASAKI, 212-8582, Japan.

09:50 **On the identification of the oxygen vacancy in HfO_2**

S J Clark[1], L Lin[2], J Robertson[2],

[1]Physics Dept, Durham University, Durham, UK, [2]Engineering Dept, Cambridge University, Cambridge CB2 1PZ, UK.

10:10 **Strain-induced ferromagnetism in $LaCoO_3$: Theory and growth on Si (001)**

A. Posadas[1], M. Berg[1], H. Seo[1], D.J. Smith[2], A.P. Kirk[3], D. Zhernokletov[3], R.M. Wallace[3], A. de Lozanne[1], and A.A. Demkov[1]

[1]Department of Physics, The University of Texas at Austin, Austin, Texas, [2]Department of Physics, Arizona State University, Tempe, Arizona, [3]Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, Texas, USA.

10:30-10:50 Coffee break

Room B **Session 5b:**
Electrical characterization and models (1)

Session Chairs: D. Schroder & T. Ernst

08:30 **Three-interface pseudo-MOSFET models for the characterization of SOI wafers with ultrathin film and BOX**

N. Rodriguez[1], S. Cristoloveanu[2], M. Maqueda[1], F. Gámiz[1], F. Allibert[3]

[1]Dept. Electronics, Facultad de Ciencias, Universidad de Granada,18071 Granada, Spain, [2]IMEP-LAHC, Grenoble INP MINATEC, BP 257, 38016 Grenoble Cedex 1, France, [3]SOITEC, Chemin de Franque, Bernin, 38926 Crolles, France.

08:50 **Nanosized metal grains induced electrical characteristic fluctuation in 16-nm-gate high-k / metal Gate bulk FinFET devices**

Y. Li[1,2], H.-W. Cheng[1], C.-Y. Yiu[1], and H.-W. Su[2]

[1]Institute of Communications Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, [2]Deptartment of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

09:10 **Temperature and voltage dependences of the capture and emission times of individual traps in high-k dielectrics**

M. Toledano-Luque[1,2], B. Kaczer[2], E. Simoen[2], Ph. J. Roussel[2], A. Veloso[2], T. Grasser[3], G. Groeseneken[2,4]

[1]Dpto. Física Aplicada III, Universidad Complutense de Madrid, Spain, [2]Imec, Leuven, Belgium, [3]TU Wien, Austria, [4]KU Leuven, Belgium.

09:30 **Interface states characterization in heterojunction solar cells from C(V) G(V) measurements and modeling**

X. Garros[1], G. Reimbold[1], J. Cluzel[1], D. Muñoz[2], P-J. Ribeyron[2]

[1]CEA-Leti/Minatec, 17 rue des Martyrs, Grenoble, France, [2]CEA-INES, 50 avenue Lac Léman, Le Bourget Du Lac, France.

09:50 **Towards barrier height modulation in HfO_2/TiN by oxygen scavenging - Dielectric defects or metal induced gap states?**

L. Pantisano[1,2], V.V.Afanas'ev[3], S.Cimino[2], C.Adelmann[1], L.Goux[1], YY.Chen[1,3], J.A.Kittl[1], D.Wouters[1,3], M.Jurczak[1]

[1]IMEC, Kapeldreef 75, B-3001 Leuven (Belgium), [2]Department of Nanobio Materials and Electronics, Gwangju Institute of Science and Technology, Gwangju (Rep. of Korea), [3]Catholics University of Leuven, Leuven, Belgium.

10:10 **Evaluation of the N- and La-induced defects in the high-k gate stack using low frequency noise characterization**

C.D. Young[1], D. Veksler[1], S. Rumyantsev[2], J. Huang[1], H. Park[1], W. Taylor[1], M. Shur[2] and G. Bersuker[1]

[1]SEMATECH, Albany, NY, USA, [2]Rensselaer Polytechnic Institute, Troy, NY, USA.

10:30-10:50 Coffee break

Room A Session 6a: Gate Stacks (Hf-based)

Session Chairs: O. Engström & C. Le Royer

10:50 **Understanding reversal effects of metallic aluminium introduced in HfSiON/TiN PMOSFETs**

S. Baudot[1], C. Leroux[2], F. Chave[1], R. Boujamaa[1], E. Martinez[2], P. Caubet[1], M. Silly[3], F. Sirotti[3], G. Reimbold[2], G. Ghibaudo[4]

[1]STMicroelectronics, 850, rue Jean Monnet, 38926, Crolles cedex, France, [2]CEA-LETI Minatec Campus, 17 rue des Martyrs, 38000 Grenoble, France, [3]Synchrotron SOLEIL, L'orme des merisiers, 91191 Gif-sur-Yvette, France, [4]IMEP-LAHC, 3, Parvis Louis Néel, 38016 Grenoble, France.

11:10 **A low gate leakage current and small equivalent oxide thickness MOSFET with Ti/HfO_2 high-k gate dielectric**

C. H. Fu, K. S. Chang-Liao, Y. A. Chang, Y. Y. Hsu, T. H. Tzeng, T. K. Wang, D. W. Heh[a], P. Y. Gu[b], and M. J. Tsai[b]

Department of Engineering and System Science, National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C. [a]National Nano Device Laboratories, Hsinchu 30078, Taiwan, R.O.C., [b]Electronics and Opto-electronics Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan, R.O.C.

11:30 **Epitaxial strontium oxide layers on silicon for gate-first and gate-last TiN/HfO_2 gate stack scaling**

M. M. Frank[1], C. Marchiori[2], J. Bruley[1], J. Fompeyrine[2], V. Narayanan[1]

[1]IBM T.J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY 10598, USA, [2]IBM Research – Zurich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland.

11:50 INVITED: **Ultrathin EOT high-k/metal Gate devices for future technologies: challenges, achievements and perspectives**

L.-Å. Ragnarsson, T. Chiarella, M. Togo, T. Schram, P. Absil, T. Hoffmann

Imec, Kapeldreef 75, BE-3001, Belgium.

12:30-14:00 Lunch

Room B Session 6b: Electrical characterization and models (2)

Session Chairs: K.L. Pey & G. Ghibaudo

10:50 INVITED: **Radiation effects in new materials for nano-devices**

R. D. Schrimpf[1], D. M. Fleetwood[1], M. L. Alles[1], R. A. Reed[1], G. Lucovsky[2] and S. T. Pantelides[1]

[1]Vanderbilt University Nashville, TN 37212 USA, [2]North Carolina State University Raleigh, NC 27695 USA.

11:30 **Performance of (110) P-channel SOI-MOSFETs fabricated by deep-amorphization and solid-phase epitaxial regrowth processes**

A. Ohata[a], Y. Bae[b], T.Signamarcheix[d], J. Widiez[d], B.Ghyselen[e], O.Faynot[d], L. Clavelier[d], S. Cristoloveanu[c]

[a]Department of Electrical Engineering, Osaka City University, Japan, [b]Department of Electronics, Uiduk University, Korea, [c]IMEP-LAHC, Grenoble INP Minatec, France, [d]CEA-LETI-MINATEC, France, [e]SOITEC, France.

11:50 **Interface traps and random dopants induced characteristic fluctuations in emerging MOSFETs**

Y. Li[1,2], H.-W. Cheng[1], and Y.-Y. Chiu[1]

[1]Institute of Communications Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, [2]Deptartment of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

12:10 **Grain boundary mediated leakage current in polycrystalline HfO_2 films**

K. McKenna[1,2], A. Shluger[1,2], V. Iglesias[3], M. Porti[3], M. Nafría[3], M. Lanza[3] and G. Bersuker[4]

[1]World Premier International Research Center, Advanced Institute for Materials Research, Tohoku University, 2-1-1, Katahira, Aoba-ku, Sendai 980-8577, Japan, [2]Department of Physics and Astronomy, University College London, Gower Street, London WC1E 6BT, [3]Dept. Enginyeria Electrònica, Universitat Autònoma de Barcelona, Edifici Q, 08193 Bellaterra, Spain, [4]SEMATECH, Austin, 78741 TX, USA.

12:30-14:00 Lunch

Room A Session 7a: Gate Stacks (Alternative materials)

Session Chairs: J. Fompeyrine & C. Leroux

14:00 **$LaScO_3$ as a higher-k dielectric for p-MOSFETs**

E. Durğun Özben[1], M. Schnee[1], A. Nichau[1], V. Mussmann[1], R. Lupták[1], J. M. J. Lopes[1,3], St. Lenk[1], K. K. Bourdelle[2], Q. T. Zhao[1], J. Schubert[1], S. Mantl[1]

[1]Peter Grünberg Institute 9 (PGI-9-IT) and JARA-FIT, Research Center Jülich, D-52425 Jülich, Germany, [2]SOITEC, Parc Technologique des Fontaines, 38190 Bernin, France.

14:20 **Phase stabilization of sputtered strontium zirconate**

M. Grube[1], D. Martin[1], W. M. Weber[1], T. Mikolajick[1,2] and H. Riechert[3]

[1]Namlab gGmbH, Nöthnitzer Strasse 64, 01178 Dresden, Germany, [2]Chair of Nanoelectronic Materials, University of Technology Dresden, 01062 Dresden, Germany, [3]Paul Drude Institute for Solid State Electronics, 10117 Berlin, Germany.

14:40 **Effect of thin Si insertion at metal gate/high-k interface on electrical characteristics of MOS device with La_2O_3**

D. Kitayama, T. Koyanagi, K. Kakushima*, P. Ahmet, K. Tsutsui*, A. Nishiyama*, N. Sugii*, K. Natori, T. Hattori and H. Iwai

Frontier Research Center, Tokyo Institute of Technology, *Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan.

15:00 INVITED: **Ternary rare-earth oxides on Si and higher mobility substrates and their integration as high-k gate dielectrics in MOSFET devices**

J. Schubert

Peter Grünberg Institute 9 (PGI-9-IT) and JARA-FIT, Research Center Jülich, D-52425 Jülich, Germany.

Room B Session 7b: Reliability (1)

Session Chairs: E. Miranda & V. Huard

14:00 INVITED: **Physical analysis of breakdown in high-κ / metal gate stacks using TEM/EELS and STM for reliability enhancement**

K. L. Pey[a,b], N. Raghavan[a], X. Wu[a], W. Liu[a], X. Li[c], M. Bosman[d], K. Shubhakar[a], Z. Z. Lwin[a], Y. Chen[a], H. Qin[a] and T. Kauerauf[e]

*[a]School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore 639 798, [b]Singapore University of Technology and Design (SUTD), Singapore 279 623, [c]A*STAR Institute of Microelectronics (IME), Science Park II, Singapore 117 685, [d]A*STAR Institute of Materials Research and Engineering (IMRE), Singapore 117 602, [e]Interuniversity Microelectronics Centre (IMEC), 3001 Leuven, Belgium.*

14:40 **Bias dependence of PBTI degradation mechanism in metal-oxide-semiconductor field effect transistors with La-incorporated hafnium-based dielectric**

T.-Y. Jang[1], D.-H. Kim[1], J. Kim[1], J. S. Chang[1], J. K. Jeong[1], Y.-U. Heo[2], Y. K. Kim[3], C. Choi[4], H. Park[5] and R. Choi[1]

[1]Inha University, 253 Yonghyun-dong, Nam-gu, Incheon 402-751, Korea, [2]Pohang University of Science and Technology, San 31, Hyoja dang, Pohang 790-784, Korea, [3]Ulsan National Institute of Science and Technology, 100 Banyeon-ri, Eonyang-eup, Ulsan 689-798, Korea, [4]Hanyang University, 17 Haengdang, Seongdong-Gu, Seoul,133-791 Korea, [5]SEMATECH, 257 Fuller Rd, Suite 2200, Albany, NY 12203, U.S.A.

15:00 **SiON and SiO2/HfSiON Gate oxides time dependent dielectric breakdown measurements at nanoscale in ultra high vacuum**

P. Delcroix[1,2], S. Blonkowski[1], M. Kogelschatz[2], M. Rafik[1], O. Gourhant[1], D. JeanJean[1] , R. Beneyton[1], D.Roy[1], X. Federspiel[1], F. Martin[3], X. Garros[3], H. Grampeix[3], R. Gassilloud[3]

[1]STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles France, [2]LTM-UMR CNRS/UJF/INPG-CEA-LETI, 17 avenue des martyrs 38000, Grenoble, France, [3]CEA-LETI, 17 avenue des martyrs 38000, Grenoble, France.

15:20 **Initial leakage current related to extrinsic breakdown in HfO_2/Al_2O_3 nanolaminate ALD dielectrics**

C. Martínez-Domingo[1], X. Saura[1], A. Conde[1], D. Jiménez[1], E. Miranda[1], J.M. Rafí[2], F. Campabadal[2] and J. Suñé[1]

[1]Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Bellaterra, Spain, [2]Institut de Microelectrònica de Barcelona, IMB-CNM, CSIC, Bellaterra, Spain.

15:40 **Monteynard Lake Excursion and Gala Dinner**

Friday June 24, 2011

Room A Session 8a: Reliability (2)

Session Chairs: B. Kaczer & C. Young

08:50 **NBTI related time-dependent variability of mobility and threshold voltage in pMOSFETs and their impact on circuit performance**
N. Ayala[1], J. Martin-Martinez[1], E. Amat[1], M. B. Gonzalez[2], P. Verheyen[2], R. Rodriguez[1], M.
Nafria[1], X. Aymerich[1] and E. Simoen[2]
[1]Universitat Autònoma de Barcelona, Dept. Enginyeria Electrònica Edifici Q. 08193 Bellaterra (Spain), [2]Imec. Kapeldreef 75, 3001 Leuven, Belgium.

09:10 **On the impact of the Si passivation layer thickness on the NBTI of nanoscaled $Si_{0.45}Ge_{0.55}$ pMOSFETs**
J. Franco[1], B. Kaczer, M. Toledano-Luque[2], Ph. J. Roussel, P. Hehenberger[3], T. Grasser[3], J. Mitard, G. Eneman1[4], L. Witters, T. Y. Hoffmann and G. Groeseneken[1]
Imec, Kapeldreef 75, 3001 Leuven – Belgium, [1]also ESAT, Katholieke Universiteit Leuven, [2]also Dpto. Física Aplicada III, Universitad Complutense Madrid – Spain, [3]Technische Universität Wien – Austria, [4]also FWO-Vlaanderen.

09:30 **On the dynamic NBTI of the HfO_2 and HfSiON high-k gate pMOSFETS**
Y. Gao, D. S. Ang, A. A. Boo and Z. Q. Teo
Nanyang Technological University, School of Electrical and Electronic Engineering, Singapore 639798.

09:50 INVITED: **From defects creation to circuit reliability –A bottom up approach**
V. Huard[1], F. Cacho[1], Y. Mamy Randriamihaja[1,2] and A. Bravaix[2]
[1]STMicroelectronics, Crolles2 alliance, 850 rue Jean Monnet, 38926 Crolles, France, [2]IM2NP-ISEN, UMR CNRS 6137, Maison des Technologies, place G. Pompidou, 83000 Toulon, France.

10:30-10:50 Coffee break

Room B Session 8b: Si interface characterization

Session Chairs: V. Afanas'ev & Y. Kuk

08:30 **Nanoanalysis of a sub-nanometre reaction layer in a metal inserted high-k gate stack**
A.J. Craven[1,2], B. Schaffer[1,2] and M.C. Sarahan[1,2]
[1]Kelvin Nanocharacterisation Centre, SUPA School of Physics and Astronomy, University of Glasgow, Glasgow, G12 8QQ, Scotland, UK, [2]SuperSTEM, STFC Daresbury Laboratories, Keckwick Lane, Warrington, WA4 4AD, UK.

08:50 INVITED: **Magnetic resonance spectroscopy of defects at the dielectric-semiconductor interface: Ge substrates and Si nanowires**
M. Fanciulli[1,2], A. Molle[2], S. Baldovino[1,2], and A. Vellei[1,2]

[1]*Dipartimento di Scienza dei Materiali, Università degli Studi di Milano-Bicocca,Via R. Cozzi 53, 20125 Milano, Italy,* [2]*Laboratorio MDM, IMM-CNR, Via C. Olivetti 2, 20041 Agrate Brianza (MB), Italy.*

09:30 **Inherent interfacial Si dangling bond point defects in thermal (110) Si/SiO_2**

K. Keunen, A. Stesmans, and V. V. Afanas'ev
Department of Physics, and INPAC-Institute for Nanoscale Physics and Chemistry, University of Leuven, Celestijnenlaan 200 D, 3001 Leuven, Belgium.

09:50 **Study of interfaces and band offsets in TiN/amorphous $LaLuO_3$ gate stacks**

I.Z. Mitrovic[1], G. Simutis[2], W.M. Davey[1], N. Sedghi[1], S. Hall[1], V.R. Dhanak[2], I. Alexandrou[3], Q. Wang[4], J.M.J. Lopes[5], J. Schubert[5]
[1]*University of Liverpool, Department of Electrical Engineering & Electronics, Brownlow Hill, Liverpool L69 3GJ, UK,* [2]*University of Liverpool, Department of Physics, Brownlow Hill, L69 7ZD, UK,* [3]*NanoPort FEI COMPANY, Building AAE-III-0-075, Achtseweg-noord 5, 5651 GG Eindhoven, The Netherlands,* [4]*King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia,* [5]*Peter Grunberg Institute PGI-9, and JARAFIT, Research Centre Julich, D-52425 Julich, Germany.*

10:10 **Charge trapping and interface characteristics in normally-off Al_2O_3/GaN-MOSFETs**

K.-W. Kim, S.-D. Jung, D.-S. Kim, K.-S. Im, H.-S. Kang, and J.-H. Lee, Y. Bae[1], D.-H. Kwon[2], S. Cristoloveanu[3]
School of Electronic Engineering & Computer Science, Kyungpook National University, Daegu, 702-701, Korea, [1]*Department of Electronics Engineering, Uiduk University, Gyeongju, 780-713, Korea,* [2]*School of Electronic Information and Communication Engineering, Kyungil University Gyeongsan, 712-701, Korea,* [3]*IMEP, Grenoble Polytechnic Institute, Minatec, Grenoble, France*

10:30-10:50 Coffee break

Room A Session 9a: Theory (2)

Session Chairs: M. Fanciulli & P. Blaise

10:50 **Charge trapping in substoichiometric germanium oxide**

J. F. Binder, P. Broqvist, A. Pasquarello
Chaire de Simulation à l'Echelle Atomique (CSEA), Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland.

11:10 **Ge-related impurities in high-k oxides: carrier traps and interaction with native defects**

E. Golias[1,2], L. Tsetseris[1], and A. Dimoulas[2]
[1]*Department of Physics, National Technical University of Athens, GR-15780 Athens, Greece,* [2]*MBE Laboratory, NCSR Demokritos, GR-15310 Athens, Greece.*

11:30 **Identification of defect levels at $In_xGa_{1-x}As$/oxide interfaces through hybrid functionals**
H.-P. Komsa, A. Pasquarello
Chaire de Simulation à l'Echelle Atomique (CSEA), Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland.

11:50 INVITED: **Defect gap states on III-V semiconductor – oxide interfaces**
J. Robertson and L. Lin
Engineering Department, University of Cambridge, Cambridge CB2 1PZ, UK.

12:30-14:00 Lunch

Room B Session 9b: Back end materials and MIM

Session Chairs: R. Schrimpf & L.A. Ragnarsson

10:50 INVITED: **MIM in 3D: dream or reality?**
J.H. Klootwijk[1], K.B. Jinesh[2], F. Roozeboom[3]
[1]Philips Research Europe, High Tech Campus 4, NL-5656 AS Eindhoven, The Netherlands, [2]Energy Research Institute, Nanyang Technological University, Singapore, [3]Eindhoven University of Technology, PO Box 513, NL-5600 MB Eindhoven and with TNO, Eindhoven, The Netherlands.

11:30 **Electron spin resonance study of defects in low-k oxide insulators (k=2.5 – 2.0)**
V. V. Afanas'ev[1], K. Keunen[1], A. Stesmans[1], M. Jivanescu[1], Zs. Tőkei[2], M. R. Baklanov[2], and G. P. Beyer[2]
[1]Department of Physics and Astronomy, University of Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium, [2]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium.

11:50 **Electrical properties of TiO2-based MIM capacitors deposited by $TiCl_4$ and TTIP based atomic layer deposition processes**
B. Hudec[1], K. Hušeková[1], A. Tarre[2], J. H. Han[3], S. Han[3], A. Rosová[1], W. Lee[3], A. Kasikov[2], S. Ji Song[3], J. Aarik[2], C. S. Hwang[3] and K. Fröhlich[1]
[1]Institute of Electrical Engineering, Slovak Academy of Sciences, Dúbravská Cesta 9, 841 04 Bratislava, Slovak Republic, [2]Institute of Physics, University of Tartu, Riia 142, 51014 Tartu, Estonia, [3]Department of Materials Science and Engineering, WCU Hybrid Materials Program, Seoul National University, Seoul, 151-744, Korea.

12:10 **Improved EOT and leakage current for metal-insulator-metal capacitor stacks with rutile TiO_2**
M. Popovici, M.-S. Kim, K. Tomida, J. Swerts, H. Tielens, A. Moussa, O. Richard, H. Bender, A. Franquet, T. Conard, L. Altimime, S. Van Elshocht, J. A. Kittl
Imec, 75 Kapeldreef, 3001 Leuven, Belgium.

12:30-14:00 Lunch

Room A Session 10a: New Devices

Session Chairs: G. Baccarani & B. Majkusiak

14:00 INVITED: **Ultra-dense silicon nanowires : a technology, transport and interfaces challenges insight**

T. Ernst, S. Barraud, K. Tachi, C. Vizioz, T. Magis, P. Brianceau, A. Hubert, N. Vulliet*, J.-M. Hartmann and M. Cassé

*CEA-LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble, France, *STMicroelectronics, 850 Rue Jean Monnet 38926 Crolles Cedex, France.*

14:40 **A FinFET memory with remote carrier trapping in ONO buried insulator**

S.-J. Chang[1], M. Bawedin[2], W. Xiong[3], S. C. Jean[4], J.-H. Lee[4], S. Cristoloveanu[1]

[1]IMEP-LAHC, Grenoble INP Minatec, BP 257, 38016 Grenoble, France, [2]IES, University of Montpellier 2, Montpellier, France, [3]SEMATEC, Austin, Texas, USA, [4]Kyungpook National University, Daegu, Korea.

15:00 **Atomic-layer-deposited Al_2O_3 and HfO_2 on GaN: a comparative study on interfaces and electrical characteristics**

Y. C. Chang[a], M. L. Huang[b], Y. H. Chang[a], Y. J. Lee[a], H. C. Chiu[a], J. Kwo[b,c], and M. Hong[a]

[a]Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan 30013, [b]Department of Physics, National Tsing Hua University, Hsinchu, Taiwan 30013, [c]Center for Condensed Matter Sciences, National Taiwan University, Taipei, Taiwan 10617.

15:20 INVITED: **Graphene: materials to devices**

J. Chae[2], J. Ha[1,2], H. Baek[1], Y. Kuk[1], S. Y. Jung[2], Y. J. Song[2], N. B. Zhitenev[2], J. A. Stroscio[2], S. J. Woo[3], Y.-W. Son[3]

[1]Department of physics and astronomy, Seoul National University, Seoul 151-747, South Korea, [2]Center for Nanoscale Science and Technology, National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20988, USA, [3]School of computational Sciences, Korea Institute of Advanced Studies, Dongdaemoon-gu, Seoul, 130-722, Korea.

16:00 **Student Award and closing**

16:10-16:30 Coffee

Room B Session 10b: Germanium

Session Chairs: A. Dimoulas & P. Hurley

14:00 **Impact of GeOx interfacial layer thickness on Al_2O_3/Ge MOS interface properties**

R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka and S. Takagi

School of Engineering, The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan.

14:20 **Remote plasma-deposited GeO_2 with quartz- like Ge- and O-local bonding: 2 band-edge state and O-vacancy comparisons with SiO_2**
G. Lucovsky, D. Zeller, K. Wu and J.L. Whitten
Depts. of Physics and Chemistry, North Carolina State Univ., Raleigh, U.S.A.

14:40 INVITED: **Interfaces & performance: what future for nanoscale Ge & SiGe based CMOS?**
C. Le Royer
CEA-LETI, Minatec campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France.

15:20 **Characterization of chemical bonding features at metal/GeO_2 interfaces by X-ray photoelectron spectroscopy**
M. Matsui[a], H. Murakami[a], T. Fujioka[a], A. Ohta[a], S. Higashi[a], and S. Miyazaki[b]
[a]Graduate School of Advanced Sciences and Matter, Hiroshima University, Kagamiyama 1-3-1, Higashi-Hiroshima 739-8530, Japan, [b]Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya, Aichi 464-8603, Japan.

15:40 **Atomic layer deposition of Al_2O_3 on S-passivated Ge.**
S.Sioncke[1], J. Ceuppens[1], D. Lin[1], L. Nyns[1], A. Delabie[1], H. Struyf[1], S. De Gendt[1,3], M. Müller[2], B. Beckhoff[2] and M. Caymax[1]
[1]Imec, Kapeldreef 75, 3001 Leuven, Belgium, [2]Physikalisch-Technische Bundesanstalt (PTB), Abbestrasse 2-12, D-10587 Berlin, Germany, [3] Also at KULeuven, Celestijnenlaan 200F, B-3001 Leuven, Belgium.

16:00 **Student Award and closing => Room A**

Posters Session

Wednesday, June 22, Lesdiguières blockhouse at La Bastille Fortress
(by cable car)

Session Chairs: I. Ionica & F. Boulanger

P1 **Atomic-layer-deposited tantalum silicate as a gate dielectric for III-V MOS devices**
C. Adelmann, D. Lin, L. Nyns, B. Schepers, A. Delabie, S. Van Elshocht, and M. Caymax
Imec, Kapeldreef 75, B-3001 Leuven, Belgium.

P2 **Duty cycle effect on barrier breakdown in MgO magnetic tunnel junctions**
S. Amara[a] , R.C. Sousa[a], J. Alvarez-Hérault[b], L. Lombard[b], H. Bea[a] , I.L. Prejbeanu[b], K. Mackay[b] and B. Dieny[a]
[a]Spintec (UMR 8191 CEA/CNRS/UJF), Grenoble, France. [b]Crocus Technology, Grenoble, France.

P3 – **CHC degradation of strained devices based on SiON and high-k gate dielectric materials**
E.Amat[1], R.Rodríguez[1], M.B.González[2], J.Martín-Martínez[1], M.Nafría[1], X.Aymerich[1], P.Verheyen[2], E.Simoen[2]
[1]Electronic Engineering Department, Universitat Autònoma de Barcelona (Spain), [2]Imec, Leuven, Belgium.

P4 – Single $SrTiO_3$ and $Al_2O_3/SrTiO_3/Al_2O_3$ based MIM capacitors: Impact of the bottom electrode material

C. Baristiran Kaynak[a], M. Lukosius[a], B. Tillack[a,b], Ch. Wenger[a], T. Blomberg[c], G. Ruhl[d]

[a]IHP, Im Technologiepark 25, 15236, Frankfurt (Oder), Germany, [b]Technische Universität Berlin, HFT4, Einsteinufer 25, 10587, Berlin, Germany, [c]ASM Microchemistry Ltd., Väinö Auerin katu 12 A, 00560 Helsinki, Finland, [d]Infineon Technologies AG, Wernerwerkstr. 2, 93049 Regensburg, Germany.

P5 Reliability and gate conduction variability of HfO_2-based MOS devices: a combined nanoscale and device level study.

A. Bayerl, M. Lanza, M. Porti, F. Campabadal[1], M. Nafría, X. Aymerich, G. Benstetter[2]

Dept. Eng. Electrònica, Universitat Autònoma de Barcelona, 08193, Bellaterra, Barcelona, Spain, [1]Institut de Microelectrònica de Barcelona, IMB-CNM, CSIC, 08193, Bellaterra, Barcelona, Spain, [2]Dept. Electrical Engineering, Deggendorf University of Applied Sciences, 94469 Deggendorf, Germany.

P6 Experimental investigation of ESD design window for fully depleted SOI N-MOSFETs

T. Benoist[1,2,3], C. Fenouillet-Beranger[2,1], P. Perreau[2,1], C. Buj[2,1], P. Galy[1], D. Marin-Cudraz[1], O. Faynot[2], S. Cristoloveanu[3], P. Gentil[3]

[1]STMicroelectronics Crolles, 850 rue Jean Monnet F-38926 Crolles Cedex, France, [2]CEA-Leti Minatec, 17 rue des Martyrs 38054 Grenoble cedex 9, France, [3]IMEP-LAHC, Grenoble INP, Minatec, 3 parvis Louis Néel, BP 257, 38016 Grenoble Cedex 1, France.

P7 Improved low frequency noise model for MOSFET operated in non-linear region

T. Boutchacha and G. Ghibaudo

IMEP-LAHC, MINATEC-INPG, BP 257, 38016 Grenoble, France.

P8 Investigation of reoxidation mechanisms in nitrided tunnel oxides for Flash memory applications.

N. Breil[1], L. Cassagnard[2], C. Arsac[2], R. Duru[2], G. Briend[1]

[1]IBM, 850 rue Jean Monnet, 38920 Crolles, France, [2]STMicroelectronics, 850, rue Jean Monnet, 38920 Crolles, France.

P9 Band offsets at Ge/GeO_2 interfaces: Effect of different interfacial bonding patterns

P. Broqvist, J. F. Binder, A. Pasquarello

Chaire de Simulation à l'Echelle Atomique (CSEA), Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland.

P10 Resistance switching in HfO_2-based OxRRAM devices

P. Calka[1], E. Martinez[1], D. Lafond[1], H. Dansas[1], S. Tirano[2], V. Jousseaume[1], F. Bertin[1], C. Guedj[1]

[1]CEA-LETI, MINATEC campus, 17 rue des martyrs, 38054 Grenoble cedex 9, France, [2]IM2NP, UMR CNRS 6242, Polytech' Marseille, Université de Provence,- 13451 Marseille Cedex 20, France.

P11 In-situ atomic layer deposition and synchrotron-radiation photoemission study of Al_2O_3 on pristine n-GaAs (001)-4×6 surface

Y. H. Chang[a], M. L. Huang[b], P. Chang[a], J. Y. Shen[a], B. R. Chen[a], C. L. Hsu[a], T. W. Pi[c],*, M. Hong[a], J. Kwo[b,d]

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P12 Interfacial reactions of Gd- and Nb-oxide based high-k layers deposited by aqueous chemical solution deposition

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P13 Low-frequency noise in SOI pseudo-MOSFET with pressure probes

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P14 New numerical low frequency noise model for front and buried oxide trap density characterization in FDSOI MOSFETs

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P15 Band alignment of Hf- Zr oxides on Al_2O_3\GeO_2\Ge stacks

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P16 Post-deposition processing and oxygen content of TiO_2-based capacitors

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P17 Improved electrical characteristics and reliability of Ge MOSFET device with nitrided high-k gate dielectric by plasma immersion ion implantation

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P18 Shallow Trench Isolation based on selective formation of oxidized porous silicon

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P19 Transport and interface states in high-k $LaSiO_x$ dielectric

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P20 Electron tunneling in MIS capacitors with the MBE-grown fluoride layers on Si(111) and Ge(111): role of transverse momentum conservation

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P21 Comprehensive studies of the degradation mechanism in amorphous InGaZnO transistors by the negative bias illumination stress

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P22 Temperature and annealing effects on InAs nanowire MOSFETs

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P23 Influence of La substitution on the electrical properties of metal-ferroelectric ($BiFeO_3$)-insulator (CeO_2)-semiconductor nonvolatile memory structures

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P24 Resistive switching characteristics of solution-processed TiO_x for next-generation non-volatile memory application; transparency, flexibility, and nano-scale memory feasibility

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P25 Performance enhancement of GaN SB-MOSFET on Si substrate using two-step growth method

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P26 Investigation of bulk defects in amorphous and crystalline HfO_2 thin films

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P27 Study on electrical characteristics and reliability of fluorinated HfO_2 for HKMG

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P28 Millisecond flash-lamp annealing of $LaLuO_3$

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P29 Atomic bonding and disorder at Ge:GeO_2 interfaces

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P30 O-vacancies in transition metal (TM) oxides: coordination and local site symmetry of transition and negative ion states in TM_2O_3 and TMO_2 oxides

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P31 Metal-Insulator-Metal capacitors with MOCVD grown Ce-Al-O as a dielectric

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P32 The influence of crystallinity on the resistive switching behavior of TiO_2

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P33 Lanthanum diffusion in the TiN/LaO_x/HfSiO/SiO_2/Si stack

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P34 Identification of electron trap location degrading low-frequency noise and PBTI in poly-Si/HfO2/interface-layer gate-stack MOSFETs

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P35 Model for the leakage current decay in high-field stressed Al/ $HfYO_x$/GaAs structures

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P36 Effect of biasing at elevated temperature on the electronic structure of Pt/HfO_2/Si stacks

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P37 Study of CVD nanowire high-k metal interface quality for interconnect level MOS devices

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P38 Epitaxy of $BaTiO_3$ thin film on Si (001) using a $SrTiO_3$ buffer layer for non-volatile memory application

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P39 Soft breakdown in irradiated high-k nanolaminates

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P40 Towards metal electrode interface scavenging of rare-earth scandates: a Sc2O3 and Gd_2O_3 study

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P41 Electronic and optical properties of hafnia polymorphs

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P42 Stability and charge transfer at the interface between SiC(0001) and epitaxial graphene

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P43 A comparative 1/f Noise study of GeOI wafers obtained by the Ge enrichment technique & the smart-cut technology

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P44 Optimization of hafnium oxide for use in nanoparticle memories

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P45 Gate-induced drain leakage in FD-SOI devices: what the TFET teaches us about the MOSFET

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P46 Impact of insertion of ultrathin TaO_x layer at the Pt/TiO_2 interface on resistive switching characteristics

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P47 MOS devices with tetragonal ZrO_2 as gate dielectric formed by annealing ZrO_2/Ge/ZrO_2 Laminate

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P48 Improved retention characteristic of charge-trapped flash device with sealing layer/Al_2O_3 or Al_2O_3/high-k stacked blocking layers

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P49 Improving electrical characteristics of W/HfO_2/$In_{0.53}Ga_{0.47}As$ gate stacks by altering deposition techniques

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