IMEP-LAHC

SEMINAIRE

(de 13 h à 14 h, salle Belledonne, IMEP, MINATEC,
ouvert aux chercheurs des autres laboratoires)

Jeudi 20 octobre 2011

"Transport characterization in 3D nanowire structure devices"

by Jae Woo, LEE

Abstract: 3D Nanowire structures come into the spotlight as next generation of FET structure. FinFETs and nanowire transistors are widely studied to be applied to the mass production.

In this presentation, we will focus on the characterization and analysis of Si FinFET and SiGe 3D stacked nanowire. Based on the low temperature measurements and mobility analysis, issues of transport mechanism of each device will be shown. Surface roughness of FinFET degrades the performance of device. Surface roughness of FinFET structure can be extracted with non-destructive method. In the case of SiGe, strain engineering is applied to enhance the mobility. The relationship between the strain and short channel effects will be discussed.

Jae Woo Lee *received the B.S. and M.S. degrees in Electrical Engineering from Korea University, Seoul, Korea, in 2006 and 2008, respectively. He is currently working toward the Ph.D. degree in international co-supervisor program with Nano Device Lab. at Korea University and IMEP-LAHC at Grenoble-INP, Grenoble, France. His main research interests include the fabrication and the characterization of nanoscale devices such as ZnO nanowire FET, SiGe nanowire FET and finFET, and also the analysis of the carrier transport mechanisms.*

Institut de Microélectronique, Electromagnétisme et Photonique
MINATEC, INPG, 3 Parvis Louis Neel, BP 257, 38016 GRENOBLE CEDEX 1, France
Tél. +33 (0) 456.529.503 - Fax. +33 (0) 456.529.501
UMR 5130 CNRS INPG UJF
Institut Polytechnique de GRENOBLE